Amendments to the Specification

Please replace the title with the following amended title:

~~SEMICONDUCTOR DEVICE~~ TEMPERATURE DETECTION FROM DIFFERENCES IN OFF LEAK CURRENTS OF NMOS AND PMOS TRANSISTORS ON CPU CHIP

Please replace the paragraph beginning on page 1, line 30 with the following amended paragraph:

There is another prior art wherein a forward current is supplied from a constant current source by a PN ~~juncture~~ junction diode, and voltages at both ends of the diode are measured at that time, thereby measuring a temperature utilizing a relation between the voltage and the temperature (see, e.g. JP-A 5-283749).

Please replace the paragraph beginning on page 3, line 10 with the following amended paragraph:

Fig. 1 is a circuit diagram of a temperature detection circuit according to a first embodiment of the invention, wherein depicted by TRp is a p-channel MOS (PMOS) transistor and TRn is an n-channel MOS (NMOS) transistor. An input signal EN1 [[ENI]] is connected to a gate of a PMOS transistor TRp11 and a gate of an NMOS transistor TRn12, and a reset signal RESET1 is connected to a gate of the NMOS transistor TRn13. Further, a node C1 (also called as a live node) is a junction

between a drain of the PMOS transistor TRp11 and a drain of the PMOS transistor TRn13 and it is connected to a gate of an NMOS transistor TRn14. A source of the PMOS transistor TRp11 is connected to a power supply potential VDD. The NMOS transistor TRn12 is connected to a drain of the NMOS transistor TRn14 at its source, and to an output node OUT1 at its drain. A source of the NMOS transistor TRn14 is connected to a grounding potential GND. A PMOS transistor TRp15 is connected to the power supply potential VDD at its source, and to the output node OUT1 at its drain, and to a pre-charge signal PRE1 at its gate. Further, a data holding circuit structured by inverter circuits INV11 and INV12 is connected to the output node OUT1. The dimensions of the inverter are smaller than the dimensions of the NMOS transistor TRn12, the NMOS transistor TRn14 and the PMOS transistor TRp15.

Please replace the paragraph beginning on page 3, line 31 with the following amended paragraph:

When the pre-charge signal PRE1 renders the PMOS transistor TRp15 conductive at "L" level, and pre-charges the node OUT1 with "H" [["L"]] level, while the input signal EN1 is [["H"]] "L" level and the reset signal RESET1 is "L" level, so that the PMOS transistor TRp11 is rendered in ON state and the NMOS transistor TRn13 is rendered in OFF state, and the node C1 is charged with "H" level. As a result, the NMOS transistor TRn12 is rendered in OFF state and the NMOS transistor TRn14 is rendered in ON state so that the output node OUT1 [[OUT]] is held at "H" level.

Please replace the paragraph beginning on page 5, line 21 with the following amended paragraph:

As mentioned above, the CPU reads out the potential of the output node OUT1 via the control circuit 14, and when the [[CPA]] CPU detects the change of the potential from "H" level to "L" level, it can stop the system after storing these data in a safe place before these data are broken owing to overdrive thereof by heat and the like. After stopping the system, the CPU initializes the circuit during the time interval F, so that the temperature detection circuit can detect again the temperature.

Please replace the abstract with the following amended abstract:

A temperature detection circuit is provided inside a chip which is the same in which [[as]] a CPU is provided, and ~~it comprises~~ includes a temperature detection part ~~comprised of~~ having a PMOS transistor and an NMOS transistor connected in series between a power supply potential VDD and a grounding potential[[,]] ~~wherein a~~. A stray capacitance between a junction (live node) between the PMOS transistor and the NMOS transistor, and the grounding potential, is charged with a current differential between the off leak current of the PMOS transistor and the off leak current of the NMOS transistor, thereby changing the potential of the live node[[,]] ~~and when~~. When the changed potential reaches a level of a threshold value in a given period of time, it is decided that the temperature of the CPU reaches a set temperature.